LOW RESISTANCE T-GATE MOSFET DEVICE USING A DAMASCENE GATE PROCESS AND AN INNOVATION OXIDE REMOVAL ETCH

ABSTRACT OF THE DISCLOSURE

The present invention provides a method for fabricating low-resistance, sub-0.1 μm channel T-gate MOSFETs that do not exhibit any poly depletion problems. The inventive method employs a damascene-gate processing step and a chemical oxide removal etch to fabricate such MOSFETs. The chemical oxide removal may be performed in a vapor containing HF and NH_3 or a plasma containing HF and NH_3.